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09/893,032	06/26/2001	Naoyuki Ogino	81784.0239	3402

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HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2188	10

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,032	OGINO, NAOYUKI	
	Examiner	Art Unit	
	Midys Inoa	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 and 5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Language

1. Claims 2, 5-9 and 15 contain "intended use" functionality language such as: "signal processing circuit **for** processing", "CD-ROM decoder **for** decoding", "anti-shock controller **for** causing", "MP3 decoder **for** decoding", "selection circuit **for** selecting", "CD-ROM decoder **for** writing", "first arbiter **for** generating", "second arbiter **for** generating", "control circuit **for** outputting", and "counter **for** generating".

Applicant is advised that "intended use" language in the claims does not add any patentable weight. If applicant's intention is to claim the functional language, applicant is advised to change "signal processing circuit **for** processing" to "signal processing circuit processing", "CD-ROM decoder **for** decoding" to "CD-ROM decoder decoding", "anti-shock controller **for** causing" to "anti-shock controller causing", "MP3 decoder **for** decoding" to "MP3 decoder decoding", "selection circuit **for** selecting" to "selection circuit selecting", "CD-ROM decoder **for** writing" "CD-ROM decoder writing", "first arbiter **for** generating" to "first arbiter generating", "second arbiter **for** generating" "second arbiter generating", "control circuit **for** outputting" to "control circuit outputting", and "counter **for** generating" to "counter generating".

Claims 10-14 and 16-18 have the same deficiencies as those claims that they depend from.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 7-8, and 10-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. (5,818,801).

Regarding Claims 7 and 10, Watanabe et al. a signal processing circuit for processing a signal reproduced from a CD in which a CD-ROM data or CD-DA data (audio data) 12 is written comprising: a memory (buffer RAM 17); a CD-ROM decoder 20 for writing, when the CD from which the signal is to be reproduced is a CD-ROM, incoming CD-Rom data into said memory 17, and decoding said CD-ROM data while reading out the CD-ROM data from said memory (see Figure 6); an anti-shock controller 20 for causing, when the CD from which the signal is to be reproduced is a CD-DA, a predetermined amount of incoming CD-DA audio data to be stored in said memory, and reading and outputting the audio data from said memory, so that continuous output can be achieved even when the incoming audio data is interrupted (Column 7, lines 28-49); a first arbiter (digital signal processor 15) for generating an output signal for controlling said memory according to a request signal from said CD-ROM decoder; a second arbiter (digital signal processor 15) for generating an output signal for controlling said memory according to a request signal from said anti-shock controller; and a selection circuit (control microcomputer 18) for selecting an output signal from said first or second arbiter; wherein an output signal from said first arbiter is selected by said selection circuit when the CD from which the signal is to be reproduced is a CD-ROM, and, when the CD from which the signal is to be reproduced is a CD-DA, an output signal from said second arbiter is selected by said selection circuit (Column 8, lines 6-39). In the system of Watanabe et al. the decoder 20 **has both the function of shockproof control of audio data ("anti-shock controller") and error correction of CD-**

ROM data ("CD-ROM decoder"); the system does not perform the shockproof operation and the error correction operation simultaneously, thus allowing the shockproof function and the error correction function to **share the buffer RAM 17 ("memory") in their operation.** Additionally, the **digital signal processor 15 acts as both a first and second arbiter since it generates sub-code identifying the type of CD being used (CD-ROM or CD-DA),** it sends the sub-code to **the control microcomputer 18** which uses the sub-code to send a control signal to the CD-ROM decoder 20, thus **deciding whether this component will take on the function of "CD-ROM decoder" or "anti-shock controller".** When the digital signal processor sends sub-code for a CD-ROM, it is acting as a first arbiter; when the digital signal processor sends sub-code for a CD-DA, it is acting as a second arbiter.

Regarding Claims 8 and 14, Watanabe et al. teaches the signal processing circuit of claim 7, further comprising an access control circuit (control microcomputer 18) for outputting to said memory, based on the selected signal, at least an address signal for said memory, a write enable signal, and a read enable signal (see Figure 6). In this system, **the control microcomputer 18 serves the roles of selection circuit as well as access control circuit.** Once it sends the control signal to the CD-ROM decoder identifying which functions this component will perform, it also enables the writing of data and reading of data from the buffer memory 17 (Column 8, lines 6-39). It is understood that **for the writing and reading of data to occur, write/read enable signals must be present**. Any other signals necessary for access into the memory must also be present (CAS and RAS signals).

Regarding Claim 11, the access control circuit (control microcomputer 18) receives as input address data the sub-code related to the CD-ROM or CD-DA which in turn is used to

determine what type of signals will be sent to the buffer memory 17 and the decoder 20 (Column 8, lines 6-39).

Regarding Claim 12, one of the CD-DA data or the CD-ROM data is supplied to the system of Watanabe et al. via a data input circuit (CD Pickup 11, Figure 6).

Regarding Claim 13, the system of Watanabe et al. stores the data in the buffer memory 17 through the use of a DSP interface circuit 20c. At this time, it is understood that the data transmission includes a sub-code since this sub-code was previously transmitted from the digital signal processor 15 to the control microcomputer 18 in the same manner. Additionally, the data in the buffer RAM is subjected to error correction by the error correcting circuit 20b, at which point it is understood that some king of error indication must exist (error flag).

Regarding Claim 16, Watanabe et al. teaches that in switching between CD-DA data and CD-ROM data, the data written before the switch is overwritten by data after the switch. The system of Watanabe et al. does not perform the shockproof operation for the CD-DA data and the error correction operation for the CD-ROM data simultaneously; it allows the shockproof function and the error correction function to share the buffer RAM 17 ("memory") in their operation (Column 8, lines 40-58). Therefore, it is understood that once one of the two functions is complete, the buffer memory dedicates itself to the completion of the other function and thus, replaces data from the first function with data from the current function.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (5,818,801) in view of Lee (6,292,440).

Regarding Claims 9, 5, and 17-18, Watanabe et al. teaches the invention set forth by claim 7 above. Watanabe et al. does not teach an MP3 decoder for decoding data encoded in MP3 format and output from the CD-ROM decoder in MP3 format. Lee teaches an MP3 car player which has the ability to read both CDs and MP3 CD-ROMs using a file type detector 100, which determines what is the file format of the audio file. If the file format is determined to be MP3, the file goes through an MP3 file input unit and an MP3 decoder. Once it has been decoded through the MP3 decoder the file is passed through the A/D converter ("CD-ROM decoder") allowing the data to be outputted through a speaker (See Figure 1, Abstract, and column 1, lines 48-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the MP3 decoder to the system of Watanabe et al. in order to give this audio system the ability to read MP3 audio files and thus, making it a more complete system for an user to enjoy. It is understood that in integrating an MP3 decoder to the invention, the MP3-decoder would operate similar to the operation of the CD decoder and thus, it would be supplied with data from the buffer memory 17. Additionally, the arbiter of the invention would generate a signal representative of MP3 data.

Regarding Claim 6, Watanabe discloses a control microcomputer ("selection circuit"), which controls and enables the functions of the CD-ROM decoder and the shockproof controller (see figure 6 and column 8, lines 6-38). It would have been obvious to allow the control

microcomputer of Watanabe to control the function of the MP3 decoder in order to keep the system orderly by controlling of all system functions from one main controller.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (5,818,801) in view of Microsoft Dictionary. Watanabe et al teaches the invention as set forth by claim 8 above. Watanabe does not teach generating a refresh timing of the memory. Microsoft dictionary discloses a refresh cycle in which repeated electric pulses are provided to a dynamic RAM in order to renew the stored electric charges in the location containing a binary 1. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the refresh cycle of Microsoft Dictionary with the system of Watanabe et al. because, due to the simplicity and large capacity of dynamic RAMs, the buffer RAM of Watanabe et al. is most likely a dynamic RAM (page 159) and in the case of a dynamic RAM, refresh cycles are necessary in order to avoid data loss (page 379).

Response to Arguments

7. Applicant's arguments filed on January 2nd, 2004 have been fully considered but they are not persuasive.

Regarding the arguments for Claims 7 and 10, the system of Watanabe et al. teaches a decoder 20 having both the function of shockproof control of audio data ("anti-shock controller") and error correction of CD-ROM data ("CD-ROM decoder"); the system does not perform the shockproof operation and the error correction operation simultaneously, thus allowing the shockproof function and the error correction function to share the buffer RAM 17 ("memory") in their operation. Additionally, the digital signal processor 15 acts as both a first and second arbiter since it generates sub-code identifying the type of CD being used (CD-ROM or CD-DA),

it sends the sub-code to the control microcomputer 18 which uses the sub-code to send a control signal to the CD-ROM decoder 20, thus deciding whether this component will take on the function of "CD-ROM decoder" or "anti-shock controller". When the digital signal processor sends sub-code for a CD-ROM, it is acting as a first arbiter; when the digital signal processor sends sub-code for a CD-DA, it is acting as a second arbiter.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa

Midys Inoa
Examiner
Art Unit 2188

MI

Mano Padmanabhan 3/19/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
TC 2100